**LISTING OF THE CLAIMS:**

The claims are unchanged from those previously presented, although the margins and the division of the elements of claim 51 into individual lines has been somewhat rationalized.

(Claims1-39 have been cancelled.)

40.(Previously Presented) A method comprising:

receiving an address at each of a plurality of memory chips, the plurality of memory chips including a first memory chip having a first programmable code and a second memory chip having a second programmable code, wherein the first programmable code is different from the second programmable code;

enabling the first memory chip based on a comparison of a portion of the received address with the first programmable code; and

disabling the second memory chip based on a comparison of the portion of the received address with the second programmable code.

41.(Previously Presented) The method of claim 40 wherein enabling the first memory chip based on a comparison of a portion of the received address with the first programmable code includes comparing two or more bits of the received address with the first programmable code.

42.(Previously Presented) The method of claim 40 wherein enabling the first memory chip based on a comparison of a portion of the received address with the first programmable code includes comparing the portion of the received address with a selection logic circuit.

43.(Previously Presented) The method of claim 40 including comparing the portion of the received address with a first selection logic circuit of the first memory chip and with a second selection logic circuit of the second memory chip.

44.(Previously Presented) The method of claim 40 further comprising providing the address to a memory array of each of the plurality of memory chips.

45.(Previously Presented) A method comprising:

assigning a first selection code to a first memory chip and a second selection code to a second memory chip, wherein the second selection code differs from the first selection code;

receiving a portion of an address at the first memory chip and at the second memory chip;

comparing the portion of the address to the first selection code and to the second selection code; and

enabling the first memory chip and disabling the second memory chip based on the comparison.

46.(Previously Presented) The method of claim 45 further comprising receiving the address at a first memory array of the first memory chip and at a second memory array of the second memory chip.

47.(Previously Presented) The method of claim 45 wherein assigning includes coupling a bonding pad to a voltage level.

48.(Previously Presented) The method of claim 45 wherein assigning includes setting a programmable link.

49.(Previously Presented) The method of claim 45 wherein enabling the first memory chip and disabling the second memory chip based on the comparison includes enabling the first memory chip when the first selection code matches the portion of the address and disabling the second memory chip when the second selection code differs from the portion of the address.

50.(Previously Presented) The method of claim 45 wherein assigning the first selection code to the first memory chip and the second selection code to the second memory chip includes assigning the first selection code to the first memory chip and separately assigning the second selection code to the second memory chip.

51.(Previously Presented) A method comprising:

coupling a plurality of address lines of a first memory chip in parallel with a plurality of address lines of a second memory chip;

setting a first code at the first memory chip;

receiving a portion of an address at the first memory chip;

enabling the first memory chip if the received address portion matches the first code; and

otherwise disabling the first memory chip.

52.(Previously Presented) The method of claim 51 wherein enabling the first memory chip includes disabling the second memory chip.

53.(Previously Presented) The method of claim 51 further including coupling a plurality of data lines of the first memory chip in parallel with a plurality of data lines of the second memory chip.

54.(Previously Presented) The method of claim 51 further comprising setting a second code at the second memory chip independent of the first code.